#12/Response 2816 9.29.01 C.Wills

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

SHINOZAKI

Serial Number: 09/385,014 Group Art Unit: 2816

Filed: August 27, 1999 Examiner: D. LE

For: INPUT CIRCUIT HAVING CURRENT REGULATING TRANSISTOR

54990
320/162

RESPONSE UNDER 37 C.F.R. § 1.121

Commissioner for Patents
Washington, D.C. 20231

Date: September 26, 2001

Sir:

The Office Action dated June 26, 2001, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 6-20 are allowed, and therefore claims 1-5 are respectfully submitted for consideration.

As a preliminary matter, Applicant notes that USPTO Paper No. 12 entitled "Office Action Summary" indicated the status of the Office Action as being "Final". However, page 2 of the Office Action noted that the Office Action is a "Non-Final Rejection". Given the above inconsistencies, Applicant submits that the "Final" status noted in the Office Action Summary is improper. Rather, Applicant submits that the status of the Office Action is indeed "Non-Final" as correctly indicated on page 2 of the First Office Action. Accordingly, Applicant respectfully requests that the "Final" status be withdrawn.

Applicant appreciates the indication of allowance of claims 6-20. Claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by Manohar et al. (U.S. Patent No.

5,963,053, hereinafter "Manohar"). Applicant respectfully traverses this rejection, and submits that claim 1 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Claim 1, upon which claims 2-5 are dependent, recites an input circuit comprising a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal. The sources of the first and second transistors are connected in common, and the differential circuit generates an internal signal in accordance with a current flowing through the first and second transistor. The input circuit further comprises a current regulating circuit connected to the differential circuit. The current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

Accordingly, the present invention provides input circuits which amplify external signals to generate internal signals having predetermined amplitudes. Furthermore, the present invention results in the advantage of having an input circuit generating internal input signals which rise and fall in response to the rising edges and the falling edges of an external input signal.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claim 1, and therefore fails to provide the advantages which are provided by the present invention.

Manohar discloses a complementary-amplifier PECL receiver. Figure 5 of Manohar discloses a N-type amplifier 50 using n-channel differential transistors, while p-type amplifier 60 uses p-channel differential transistors. Manohar also discloses RX+ and RX-

inputs which are coupled to the gates of n-channel differential transistors 56, 58 in n-type amplifier 50, and to the gates of p5 channel differential transistors 66, 68 in p-type amplifier 60. Current-mirror transistors 52, 54 are p-channel transistors in n-type amplifier 50, but current-mirror transistors 62, 64 are n-channel transistors in p-type amplifier 60. In addition, Manohar discloses node 53 which is a bias voltage set by the drain of differential transistor 56. The bias voltage of node 53 controls the current through p-channel transistors 52, 54, and the tail current n-channel tail transistor 59. This bias voltage depends on the input voltages applied to RX+ and RX-, and the sizes of all devices including transistors 52, 56, 59.

Applicant respectfully submits that each and every element recited within claim 1 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the input circuit having current regulating transistor as recited in the present application is clearly distinct from that which is illustrated in Manohar. Specifically, it is respectfully submitted that Manohar fails to disclose or suggest an input circuit comprising a current regulating circuit connected to the differential circuit as recited in the claims. As mentioned above, the present invention is directed to an input circuit that includes a current regulating circuit for increasing and decreasing an amount of the current flowing through a differential circuit in response to an internal signal directly provided to the current regulating circuit. In contrast, Manohar merely discloses a n-channel transistor 29 and differential n-channel transistors 26, 28 of Figure 1. It is respectfully submitted that the n-channel transistor 29 of Manohar is merely a constant current source having the gate connected to the gates of current mirror transistors 22, 24. It is further submitted that the n-channel transistor 29 of Manohar cannot increase and

decrease an amount of a current in response to an internal signal. Accordingly, Applicant respectfully submits that the n-channel transistor 29 of Manohar is neither comparable nor analogous to the current regulating circuit of the present invention. Therefore, Applicant respectfully submits that Manohar fails to disclose or suggest each and every element recited within claim 1 of the present application.

Claims 2-5 were rejected as being unpatentable over Manohar in view of Fernandez et al. (U.S. Patent No. 5,448,200, hereinafter "Fernandez") and Harris et al. (U.S. Patent No. 5,475,323, hereinafter "Harris"). In making this rejection, the Office Action took the position that Manohar discloses each and every element of the claimed invention with the exception of showing a delay time or a fixed current source. The Office Action cited Fernandez and Harris for curing the deficiencies which exist in Manohar. Applicant respectfully traverses this rejection, and submits that each of claims 2-5 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Fernandez discloses a differential comparator with differential threshold for local area networks or the like. Figure 1 of Fernandez discloses a differential comparator 1 with two inputs (IN+, IN-), having a master section 3 and a slave section 2. The master section 3 (having an output TSET and having inputs coupling to fixed biases $V_c+\Delta/2$, $V_c-\Delta/2$), where A is the differential threshold value for the comparator. The slave section (responsive to the two comparator inputs IN+, IN- and to the output TSET of the master section) compares signals on the two comparator inputs and produces an output (OUT+, OUT-) when the signals differentially exceed the differential threshold value. A signal on OUT+ is asserted when a signal on IN+ exceeds a signal IN- by Δ and a signal on OUT- is asserted when the signal IN- exceeds the signal IN+ by Δ.

Harris discloses an integrated circuit apparatus and method providing for utilizing voltage dividers and differential amplifiers. Harris also discloses three integrated circuit resistors R_1, R_2 and R_3. The resistors have a L_1, L_2 and L_3, and width W_1, W_2 and W_3, respectively. The voltage drop between node 101 and node 100 is Vin, the voltage drop between node 102 and node 100 is $Vout_1$, and the voltage drop between node 103 and node 100 is $Vout_2$. Harris further discloses a microelectronic resistor voltage divider 20 with linearly spaced output taps. In order to contact the voltage divider 20, accessible outputs or tap connections are provided. Adding taps to voltage divider 20 will result in the creation of parasitic tap resistance between tap connection sites 28 and 30 and main body 34 of voltage divider 20. The effect of a tap is to place parasitic resistors, r_t associated with tap in parallel with small resistor segments, r_a, of the body of the resistor that is affected by r_t. Additionally, Harris discloses that signal distortion problems due to a common mode signal are minimized through the use of common mode feedback control circuitry 912. Common mode feedback control circuitry 912 is also connected to current sources 900 and 902 and senses the currents at nodes 914. In response to the sensed currents, common mode feedback control circuitry adjusts a variable current source 906. Variable current source 906 sinks a varying current to V_{ssa} such that the current through transistors 1000 and 1010 is maintained at constant I_D even under common mode signal conditions and independent of variations in the current source.

Applicant respectfully submits that each and every element recited within each of claims 2-5 is neither disclosed nor suggested by the combination of prior art references. In particular, each of claims 2-5 depends from independent claim 1, and therefore each and every limitation recited within claim 1 is also recited within each of claims 2-5. Therefore,

each of claims 2-5 also includes the limitation of a current regulating circuit connected to the differential circuit as recited in claim 1. As discussed above, Applicant submits that Manohar fails to disclose or suggest the limitation of a current regulating circuit connected to the differential circuit as recited in claim 1. Applicant further submits that this limitation is also neither disclosed nor suggested by Fernandez. As mentioned above, Fernandez merely discloses a differential comparator that includes a master section having a differential pair 41 and a bias transistor 44 with a slave section having a differential pair 31 and a bias transistor 34. However, it is respectfully submitted that Fernandez fails to disclose or suggest a current regulating circuit that regulates the amount of current flowing through the differential circuit such that delay time between transition points of an external signal and transition points of an internal signal are the same. Furthermore, it is respectfully submitted that Fernandez does not disclose a constant current source. Accordingly, Applicant respectfully submits that Fernandez fails to cure the deficiencies which exist in Manohar because Fernandez fails to disclose or suggest the element of a current regulating circuit connected to the differential circuit as recited in the claims.

Additionally, Applicant submits that Harris also fails to cure the deficiencies which exist in Manohar, and/or a combination of Manohar and Fernandez. As mentioned above, Harris merely discloses a comparator having a constant current source 904 and a variable current source 906. However, Applicant respectfully submits that Harris fails to disclose the current regulating circuit responsive to the internal signal. It is respectfully submitted that Harris feedback control circuit 912 merely controls the variable current source 906 such that the current through transistors 1000, 1010, is maintained at a constant. It is further submitted that the objective of Harris is to maintain a current flowing through the

differential transistors 1000, 1010 at a constant by feedback control, and therefore is neither comparable nor analogous to the present invention having a uniform delay time of the rising and falling edge of internal signals relative to the external signals. Accordingly, the comparator of Harris fails to disclose or suggest a current regulating circuit as recited in the claims.

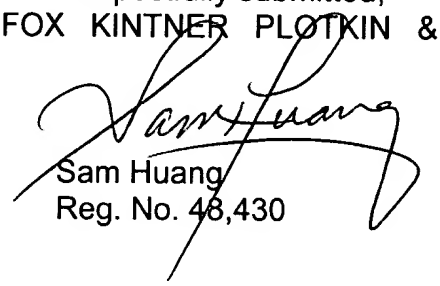
Therefore, Applicant respectfully submits that neither Manohar, nor Fernandez, nor Harris, taken alone or in combination, disclose or suggest each and every element recited within claims 2-5 of the present application.

In view of the above, Applicant respectfully submits that claims 1-5 each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 1-5 be found allowable, and that this application be passed to issue along with allowed claims 6-20.

If for any reason the Examiner determines that this application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC



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